ROD
FPGA Based Implementation of the Event Fragment Builder

December 17, 1999

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Event Fragment Builder

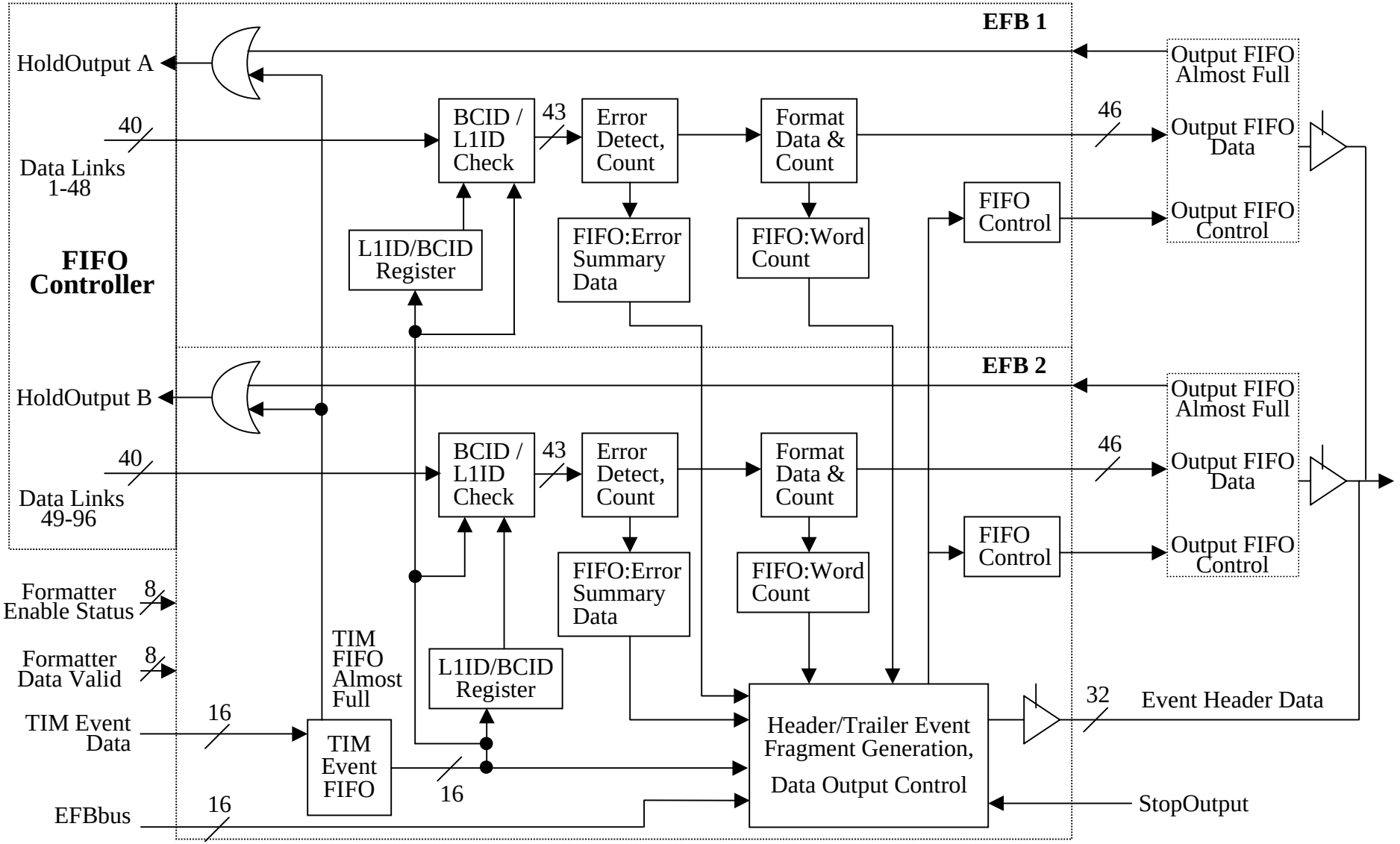
- Performs event BC/L1 ID checking, error detection and counting, and data formatting and counting.
  - Examines header and trailer to perform event ID checking and error counting.
  - Errors identified on a link-by-link basis.
  - Formats data as required by examining header and trailer of each link.

- Output to Router can be stopped.
  - If “StopOutput” is issued, data can still flow through the Event Fragment Builder and fill the output memory.

Event Fragment Builder 2

- Works on two parallel streams of data from half of the input links to mask the FIFO Controller's link-to-link latency.
  - The output FIFO memory is thus needed to de-randomize data between EFB data streams - helps achieve 40 MWords/sec bandwidth.
- Optional Features
  - Allow the debug output memories to be loaded from VME so that data patterns can be generated to test the DSPs or the Router FPGA, and supply events over the S-Link.
  - Word counts can go into event fragment header rather than the trailer if requested.

Event Fragment Builder FPGA Design



Event Fragment Builder - Functional Blocks

- BC ID / L1 ID Check:
  - Compares expected BC/L1 ID with the decoded data and flags any errors.
  - Valid data just passes through.
  - TIM Event FIFO provides L1/BC ID data so each Event Fragment Builder data path can work independently on different events.

- Error Detect:
  - Looks at data bit fields to identify errors.
  - Generates the error summary block for the event.

Event Fragment Builder - Functional Blocks 2

- Format Data and Count:
  - Removes front end trailer words unless the trailer error flag or the almost full flag was set.
  - Removes data from links with no hit data and no errors.
  - After unnecessary half words are removed, it re-packs all the data into 32 bit words so there are no gaps in the data.
  - Counts how many words were sent to the output FIFOs over an event and writes the count into a FIFO.

- Header/Trailer Block Generation, Data Output Control:
  - After the word counts are available from both Event Fragment Builders, an event is delivered to the Router.
    - An Event Header block is first transmitted to the Router.
    - Using the data counts, data is then burst from the output FIFOs.
    - Finally, the summary and event fragment trailers are transmitted.

Event Fragment Builder - Functional Blocks 3

- HoldOutput/Pause:
  - If any of the internal EFB FPGA or external output FIFOs almost full, HoldOutput will be asserted, and the FIFO controller will be told to pause.
  - Output FIFOs are big enough (16K deep) to hold largest SCT/Pixel Event.

- Stop Output:
  - If the S-Link asserts StopOutput, data will not be transmitted to the Router, but the Event Fragment Builder can still process input data and write to the output memories.

Event Fragment Builder - Design Status

- The interface specification and conceptual block diagram for the Event Fragment Builder FPGA is complete.

- VHDL code for Event Fragment Builder FPGA is 90% complete.

ROD
FPGA Based Implementation of the Router

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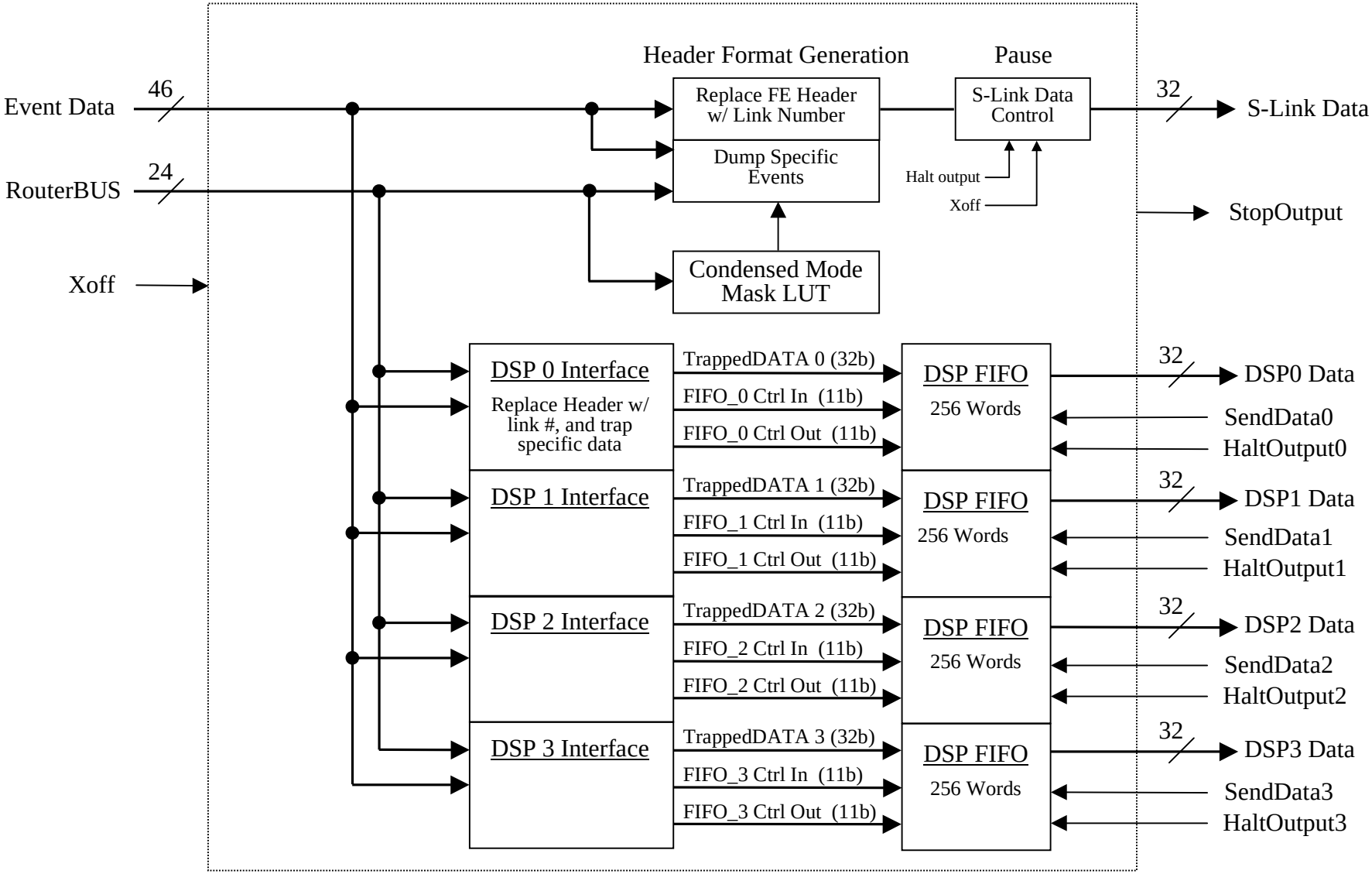
Router

- Control of Data Distribution:
  - Routes data from the Event Fragment Builder to the S-Link and the BackEnd Digital Signal Processors.
- Stop Output:
  - If the S-Link asserts Xoff, data transmission to the S-Link will stop.
  - If the DSP asserts HaltOutput, data transmission to the BackEnd DSP will stop. HaltOutput does not stop transmission to the S-Link.
- Header Format Generation:
  - Replaces FE event headers with link number information and error flags before sending event to the S-Link.

Router 2

- Dumps specific event types :
  - The type of event to be eliminated can be defined by the VME bus controller, or the ROD Controller.
- DSP Interface:
  - Router to support 4 separate DSPs with interface and FIFO memory blocks.
  - Each DSP interface can be configured to trap specific types of data.
  - DSP FIFO blocks are internal to the FPGA
- Optional Features:
  - In case of consecutive BC ID errors on one link (i.e. a missing or an extra event), a correction algorithm can be implemented.

Router FPGA Design



Router - Functional Blocks

- Header Format Generation:
  - Event from the Event Fragment Builder is routed to the S-Link and to all BackEnd DSP FIFOs.
    - The L1ID/BCID data in the FE headers is replaced with the following data:
      - The timeout flag, L1ID error flag, BCID error flag, condensed mode flag, and the link number bits.

- Stop Output:
  - If the S-Link asserts Xoff , the Router stops transmission of data to the S-Link within 2 clock cycles, and asserts StopOutput.
  - If the DSP asserts HaltOutput(n), the Router will continue data transmission to the S-Link, but will halt the specified DSP FIFO.
  - Only the S-Link is able to initiate a StopOutput in the ROD during normal data capture (run) modes.

Router - Functional Blocks 2

- DSP Interface:
  - Router to support 4 separate Slave DSPs with interface and FIFO memory blocks.
    - The board will be designed and fabricated to support 4 Slave DSPs, but only 2 modules will be loaded on this prototype. 1 DSP will be used for monitoring histograms, and the other for error checking
  - As events are captured into the DSP buffer and FIFO used for error checking , link number error status is recorded, and following the completion of all events, inserted into the Event Fragment trailer.
    - 2 bits reserved to identify errors for each link.
      - 00 = no data; 01= good data; 10 = timeout; 11 = L1ID, BCID
    - Link number error status words overwrite 3 existing trailer words.
      - Status Word Count, Data Word Count, and Status Word Position.

Router - Functional Blocks 3

- DSP Interface:
  - The error DSP interface used for error checking can be configured to trap the following data during run time.
    - Event Type
    - Error Type
    - Level 1 ID
  - Calibration
    - Only certain detector regions of interest will be calibrated at any one time.
      - Calibration of single module (subset of pixel).

Design Status

- The interface specification and conceptual block diagram for the Router FPGA is complete.

- No code has been written for the Router.